SECTION V

MINI-DISK CONTROLLER

MDIO

5 - 1 GENERAL DESCRIPTION

The MDIO is a programmable mini-floppy disk formatter/controller designed around the 1771 large scale integrated circuit. This circuit performs the various drive control and data/status transfer operations to implement the commands issued by the MDIO firmware.

MDIO firmware (2Kx8) resides on-board in a ROM/EPROM module and is accessed by the operating system through calls which follow the same conventions that govern DIO Accesses to mini-drives.

MDIO occupies 4K bytes of address space E000 - EFFF which may be released to RAM-space under system control. Within this 4K space, MDIO contains 256 bytes of on-board Ram of which the upper 128 bytes are available to the system.

Data transfer between MDIO and diskette drive occurs at 125 KHz in FM encodation. An MSI-TTL implemented data separator samples the bit stream received from the drive at a rate of 2 MHz. This provides increased reliability in data recovery.

The MDIO is structured around a internal bi-directional bus that links 1771 controller, ROM/EPROM, RAM and a memory-mapped drive-control port. This bus is connected to the DI and DO lines of the S-100 bus through a bilateral bus-switch.

5 - 2 MDIO SPECIFICATIONS

5 - 2.1 SYSTEM INTERFACE

S-100 bus compatible

IMDOS compatible (DIO access conventions)

Occupies same 4K address space as DIO

Phantom line control port switch selectable

Programmed data transfer

5 - 2.2 PERIPHERAL INTERFACE

With appropriate firmware will attach to

Shugart SA400
Shugart SA450
Wangco 82, 282
Micropolis 1015
MPI B51, B52

Selects up to 4 drives

Side select available

5 - 2.3 FORMAT AND CODING

Soft sector format, similar to IBM 3740

FM encoding, 125 KHz data rate

LSI-based formatter/controller

MSI-implemented data separator
(2 MHz bit-stream sample rate)

5 - 2.4 ELECTRICAL

On-board regulation, heatsink

VCC (+5V) 670 mA
VDD (+12V) 80mA
VBB (-5V) 50mA

Power dissipation

4.5 watts, integrated circuits
3.0 watts, regulators and miscellaneous

Open-collector drivers

peripheral interface

220/330 terminations

34-Conductor flat cable header

29 ICs; some MSI, majority SSI TTL

5 - 2.5 MDIO DRIVE SELECTION

MDIO has the capacity to select one of three mini drives.

MDIO has the hardware capability to control the side select line of two-sided mini drives, such as Shugart SA450 but IMDOS does not make use of this capability at present.

Unlike the DIO, the MDIO permits the selection and deselection of the 4K add-in space even in a megabyte, or any 65K, address space.

The MDIO is similar to the DIO in that both boards share similar designs regarding drive access.

5 - 3 FUNCTIONAL DESCRIPTION

The MDIO is designed around an LSI-chip, the 1771, which performs a majority of the mini drive control and all of the data and status transfer operations that implement MDIO firmware command sequences. These sequences, in turn, are activated by system calls requesting diskette access. The remainder of the drive control requirements are addressed by memory-mapped port.

The MDIO is organized around an on-board, bi-directional data bus that links the major components of the controller (refer to the MDIO Functional Block Diagram at the end of this section). This bus is connected to the DO and DI lines of the S-100 bus through a bi-lateral bus-switch.

Several MSI-TTL functions and a few gates form an external data separator which tracks the FM-encoded pulse stream coming from the drive during a read operation, decodes these pulses and steers separated clock and data pulses to the 1771.

A section of low-complexity combinational logic takes care of address decoding and timing requirements.

MDIO firmware resides in 2K bytes of ROM/EPROM and has available 256 bytes of RAM for variable data storage.

5 - 4 BUS ORGANIZATION

The DAL-bus (see Figure 1) is a bi-directional bus which interconnects the several MDIO components with the S-100 bus where data pathing occurs on two uni-directional buses, namely DO0 - DO7 for data transfers from CPU to peripheral and DI0 - DI7 for data transfers from peripheral to CPU. Interfacing between the DAL-bus and the DI, DO lines is accomplished by two 74LS244 bus drivers (U30 and U31).

5 – 4.1 MAJOR COMPONENTS

In addition to the bus–switch, MDIO is composed of these major functional components

- 1771 controller, a 40–pin LSI chip that supervises and directly controls communications with the selected mini drive.
- Data separator, an MSI–implemented FM pulse stream decoder interposed between the drive and the 1771.
- Memory mapped port, a six–bit strobed latch which exercises control over drive motor and side–select, as well as, drive selection in system configurations containing one or more drive(s).
- ROM/EPROM, a 24 pin device which contains the 2K bytes (optionally 1K) of MDIO firmware.
- RAM, 256 bytes of random access memory used by MDIO firmware for variable data and status storage.
- Timing and control logic, which performs address decode, bus control and device strobing functions.

Operation, with regard to device selection and access timing of the ROM/EPROM, RAM, memory–mapped port, and bus switch is straight forward and is discussed below. Operation of the 1771 and the data separator is more complex and is treated separately in Section 5 – 8.

5 – 5 MDIO ADDRESSING

The MDIO resides at E000 – EFFF within a 65K address space,, and within the highest 65K block in any configuration space that exceeds 65K. Several gates (chips U2, U15, U25 and U20) decode address lines A12 – A19 for a partial decode of MDIO board select. This decode is EXXX for an address space of 65K, FEXXX for greater than a 65K space.

The quad–XOR (U6), together with the 4–position DIP switch (SW1), a 7422 (U18), 1/4 of U9 and one D–FF (1/2 of U5) forms the control logic whereby the MDIO may be switched into and out of the address space. Execution of an OUT instruction to port NE deselects, to port NF selects the MDIO. When the MDIO is deselected, any RAM existing "behind" the MDIO becomes available to the system. The signal generated by this logic is MDIOIN.

Together with EXXX (or FEXXX), MDIOIN forms BDSELX. The X in this signal name signifies that MDIO board selection has not yet been qualified with negation of S–100 bus status signals SINTA, SINP, and SOUT. (For reasons elaborated upon in Section 5 – 6.2, these status signals are kept out of MDIO access decoding until the next logic layer.) The product of /SINTA, /SINP, and /SOUT forms the term MEM. Subsequent ANDing of BDSELX and MEM produces BDSEL. This term appears as qualifier at several nodes within the remainder of the address decode and timing logic.

MDIO RAM is located at E800 through E8FF. Access to this space is decoded by BDSEL•X8XX which produces RAMSEL (U18, U26, and U17). Similarly, ROM/EPROM resides an E000 through E7FF. Any 1K firmware will image in two regions, E000 – E3FF and E400 – E7FF, because A10 is not decoded. The standard 2K MDIO firmware will, of course, occupy the entire MDIO ROM/EPROM space. This space is distinguished from RAM space by the inversion of A11 and access is decoded by BDSEL•X(0XXX)XX which produces ROMSEL.

Located at E9X•(X1XX), the memory–mapped port is enabled by BDSEL•X9XX•A2 which forms the signal PORTSEL. SEL1771, on the other hand, is decoded by ANDing BDSELX, X9XX, and /A2. This results in the following address assignments:

memory–mapped port	E9X7
1771 data register	E9X8
1771 sector register	E9X9
1771 track register	E9XA
1771 status register	E9XB (read)
1771 command register	E9XB (write)

The DAL/S–100 bus switch is controlled by BDSEL•PDBIN for data going off–board and BDSEL•/SMEMR for data heading on–board. The control signals are OFFBRD and INBRD, respectively.

5 – 6 TIMING AND CONTROL

5 – 6.1 WRITE OPERATIONS

The S–100 bus signal /PWR is the write strobe which trips destination latches with its trailing edge during CPU to peripheral device write operations.

/PWR controls the R/W control line of RAM directly while the negation of SMEMR controls the output–disable (OD) line. During write operations, SMEMR will be low, and RAM output thus disabled (OD = 1).

/INBRD, meanwhile, will be active (/(BDSEL•/SMEMR) = 0), thus enabling data from the DO lines onto the DAL bus. At the end of /PWR, this data is latched into the RAM cell addressed by address lines A0 – A7.

Writing into the memory–mapped port occurs at the end of /PORTWT, the product of /(PORTSEL•PWR). In this case the write strobe also contains the device selection term.

The leading (i.e., falling) edge of /PORTWT triggers the DRIVE SELECT ONESHOT (1/2 of U1) which has a period of around 4 – 5 seconds. When set, the Q–output of this oneshot removes the reset on U23, thus allowing updating of the latches at the time of the trailing (i.e., rising) edge of /PORTWT.

Head loading takes place within the mini drive concurrent with drive selection. Conversely, head de–selection is equivalent to drive deselection. It follows that the head

of a selected drive will remain loaded as long as the DRIVE SELECT ONESHOT is retriggered prior to time-out.

If the oneshot is allowed to time out, the Q-output (U1-5) will revert to a low state which, in turn, resets U23. This results in drive de-selection and hence head unloading.

Since the term MOTORON is stored in an independent memory cell (FF U5), the motor(s) of the drive(s) will remain on even after DRIVE SELECT ONESHOT time-out has occurred. This ensures that the drive(s) continue at full rotational speed.

Upon drive re-selection, only the normal head load settling time will have to be reckoned with by the controller.

5 - 6.2 READ OPERATION

During read operations, /(BDSEL•PDBIN) generates /OFFBRD which enables data flow off the DAL bus and onto the DI lines. SMEMR will be high, while PWR will remain inactive.

SMEMR will thus remove the data out disable during RAM access (OD = 0) allowing the accessed RAM cell to output its contents onto the DAL bus. ROM/EPROM is enabled by /ROMSEL going true during a ROM/EPROM access.

Accessing the 1771 is a little more involved. Due to its long access time, the 1771 must be selected well in advance of strobing time at the destination (i.e., at the CPU). Similarly, the 1771 read strobe must arrive as early as possible.

This is accomplished by a) deferring the MEM qualification and deriving SEL1771 solely from address bus decoding plus MDIOIN, and b) generating an advanced "PDBIN" and qualifying that with MEM. This latter signal becomes ADVREAD, the read window for the 1771.

ADVREAD is the latched result of sampling the status line SMEMR as soon as it becomes stable on the bus. This happens to be just prior to the rising edge of PSYNC•01 in an 8080-based system and /PSYNC•01 in an 8085-based system. ADVREAD is reset by the trailing edge of PDBIN at the conclusion of the data transfer.

5 - 6.3 THE 1771 READY STATUS BIT

During initialization, the READY input of the 1771 is used to determine which of the two permissible jumpers, AG - AJ and AJ - AH, is installed on the board.

MDIO firmware strobes the control port with a dummy drive select byte that selects no drive (but does turn on drive motor(s)). This strobe fires the DRIVE SELECT ONESHOT, while also latching a "0" into 4Q at U23, thus forcing jumper point AG high.

The firmware then examines the 1771 status byte for a READY. If it finds a READY, it infers that the board is strapped for MPI B51 use and readies the appropriate parameters for step rate and number of tracks per diskette (12 ms, 40 tracks). If it finds a NOT READY, it infers that the board is not strapped for MPI B51 use and

readies the default parameters (40 ms, 35 tracks). All future control bytes strobed into U23 during drive selection activities will have bit 6 set to force a low at jumper point AG.

Before issuing a READ or a WRITE command to the 1771, MDIO firmware looks at the status of the chip to determine whether the READY flag has gone false. This flag serves the combined purpose of sensing both the readiness of a drive (where the drive does output such a status line) and the condition of the DRIVE SELECT ONESHOT.

If the firmware detects a NOT READY condition, it assumes that the oneshot has timed out. Re-selecting the specified drive will, therefore, result in the loading of the head. To allow for the required head load settling time, the firmware issues an alternate version of the READ or WRITE command which raises the HLD signal (U11-28). This fires the HEAD LOAD ONESHOT. The Q-output of this oneshot (U1-4) drives the HLT input at U11-23 low for approximately 75 ms. Sensing a low at HLT, the 1771 will defer commencement of the actual data transfer operation until HLT once again has gone high.

If, on the other hand, the firmware detects a READY condition, it will merely re-select the specified drive (thus re-firing the DRIVE SELECT ONESHOT) and issue a normal READ or WRITE command. In response to this, the 1771 assumes that the head is already loaded and begins the data transfer operation immediately.

5 - 7 PERIPHERAL INTERFACE

The MDIO interfaces with the peripheral (mini drive) through the 1771 and the memory-mapped port. The 1771 takes care of the communications protocol with the peripheral while the port provides the additional control lines not covered by the 1771. All output lines to the peripheral are driven by open collector drivers (7416).

During diskette write operations, the FM encoded serial bit stream is sourced by the 1771 directly. During diskette read operations, the encoded pulse train is separated into clock and data pulses by the data separator. These are then input to the 1771.

Much of the discussion which follows treats 1771 device characteristics in terms of its input and output pins and is derived from the functional description of the 1771-1 by National Semiconductor Corp. Detailed description of the various processes internal to the 1771 is covered in Section 5 - 8.5, titled Controller Processes.

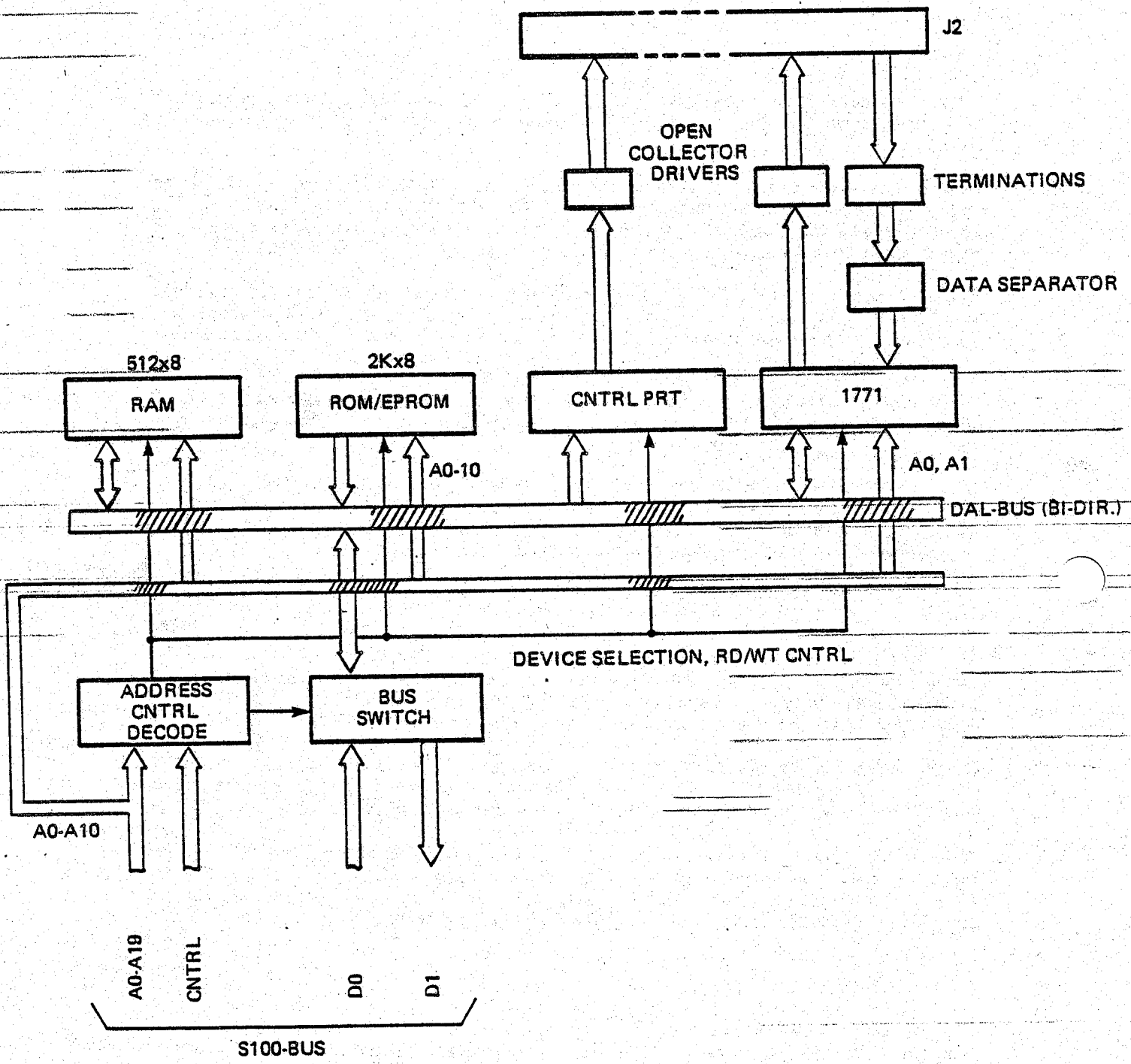
5 - 8 1771 CONTROLLER

This section summarizes the electrical characteristics of the 1771 device as well as its functional characteristics as exhibited by its input/output pin definitions. All pins are defined, and their applicability to the MDIO design clarified.

5 - 8.1 FUNCTIONAL PIN DEFINITIONS

The following describes the function of all 1771 input/output pins. Some of these descriptions reference internal circuits.

MDIO
FUNCTIONAL BLK DIAG.



NOTE: In the following descriptions, a low represents a logic 0 (0 volt nominal), and a high represents a logic 1 (+5 volts nominal).

INPUT SIGNALS

Chip Select (/CS):
When low, the chip is selected. This enables communication between the 1771-1 and the CPU.

Read Enable (/RE):
When low coincident with an active (low) /CS input, allows the CPU to read data or status information from a selected register of the chip.

Write Enable (/WE):
When low coincident with an active (low) /CS input, allows the CPU to write data or control words into a selected register of the chip.

Register Select (A0, A1) Lines:
These two inputs are used in conjunction with either an active (low) /RE or /WE input to select an 1771-1 register to read from or write into as indicated below.

A1	A0	/RE	/WE	Selected Register
0	0	0	1	Status
0	0	1	0	Command
0	1	0	1	Track
0	1	1	0	
1	0	0	1	Sector
1	0	1	0	
1	1	0	1	Data
1	1	1	0	

Master Reset (/MR):
When low, clears the Command Register, resets bit 7 (Not Ready) of the Status Register low, and makes the (/PH1)/STEP output active low. When the /MR returns high, a Restore command is executed (regardless of the state of the REady input from the floppy disk drive).

Clock (CLK):
This input pin requires a 1-megahertz (+/-1%) squarewave clock as a reference for all internal timing.

External Data Separator (/XTDS):

When low, the composite read disk serial data (data bits and clock) from the floppy disk drive is separated externally by the user. When high or open, the composite read disk data is separated by the internal data separator of the chip. This pin is tied to VSS in the MDIO.

Floppy Disk Data (FDDATA):

This input pin provides either of the following serial data: both clock and data bits (composite readdisk data) when the /XTDS input is high; or externally separated data bits when the /XTDS input is low. The latter is the mode employed in the MDIO.

Floppy Disk Clock (FDCLK):

This input pin provides the externally separated clock when the /XTDS input is low. The FDCLK input should be connected to +5 volts (logic 1) when the /XTDS input is high.

Write Protect (/WPRT):

When low, immediately terminates a Write command and sets bit 6 (Record Type/Write Protect) of the Status Register high. In addition, an interrupt is generated when the WPRT input is low. The /WPRT input is sampled whenever a Write command is received from the CPU.

Write Fault (/WF):

When low coincident with an active (high) Write Gate (WG) input, causes the current Write command to be terminated and sets bit 5 (Record Type/Write Fault) of the Status Register high. The /WF input should be made inactive (high) coincident with an inactive (low) WG input. This signal is not used in MDIO.

Index Pulse (/IP):

Goes low for 10 microseconds (minimum) whenever an index mark is encountered (once per revolution) on the diskette).

Track 00 (/TR00):

Goes low whenever the Read/Write head is positioned over track 00 of the diskette.

Ready:

When high before the execution of a Read or Write command, indicates that the floppy disk drive is ready for a Read or Write operation. When low, the Read or Write operation is not performed and an interrupt is generated. However, a Seek operation is always performed. The complement of the Ready input appears as bit 7 (Not Ready) of the Status Register. The Ready input is used for several purposes. For full description, see Section 5 – 6.3.

Three-Phase Motor Select (/3PM):

When low, the three-phase motor control interface is selected for the floppy disk drive by the 1771-1. When high or open, the step-direction motor control interface is selected by the 1771-1. This line is tied high in MDIO.

Disk Initialization (/DINT):
When low coincident with a Write Track command from the CPU, causes the Write Track operation to be terminated and bit 6 (Record Type/Write Protect) of the Status Register to be set high. This signal is not used in MDIO.

Test:
This input pin is normally tied to +5 volts. However, it may be used to disable the programmed stepping rate delays for testing the 1771-1 or for disk drives that do not require the long delay times to change tracks. These delays are disabled by tying the Test input to ground.

Head Load Timing (HLT):
When high, the Read/Write head is assumed to be engaged against the recording medium (diskette). The HLT input is sampled after each 10 millisecond internal delay.

VBB: -5 Volt supply

VCC: +5 Volt supply

VDD: +12 Volt supply

VSS: Ground (0 Volt) reference

5 - 8.2 OUTPUT SIGNALS

Data Request (DRQ):
Open-drain output to the CPU that goes high when the 1771-1 is ready to transfer a byte of data during a Read or Write operation. The DRQ output is reset low upon the completion of a byte Read or Write operation. This feature is not used on the MDIO.

Interrupt Request (INTRQ):
Open-drain output to the CPU that goes high at the completion or termination of any operation. The INTRQ output is reset low when a new command is loaded into the Command Register. This is not used in the MDIO but is brought out to a pad.

Write Data (WD):
Composite write disk data (both clock and data bits of 500 nanoseconds in duration) output to the floppy disk drive. The WD output can drive two TTL loads.

Write Gate (WG):
Active (high) whenever data is to be written on the diskette. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register (in response to a DRQ output from the 1771-1) before the WG output can be activated.

Track Greater Than 43 (TG43):

When high during a Read or Write operation, informs the floppy disk drive that the Read/Write head is positioned between tracks 44 and 76. This line is not used in the MDIO.

Three-Phase Motors/Step-Direction Motors Control Lines ((/PH1)/STEP, (/PH2)/DIRC, PH3):

These three control lines provide either of the following outputs: successive three-phase pulses (active high PH3 signal and active low /PH1 and /PH2 signals) over the lines for three-phase stepping motors; or a level over the (/PH2)/DIRC line (high level for stepping in and low level for stepping out) and 4 microsecond high-level pulses over the (/PH1)/STEP line to determine the direction and stepping rate for step-direction motors. For direction control of three-phase motors, the stepping sequence is 1-2-3-1 when stepping in and 1-3-2 when stepping out. The particular motor interface selected is determined by the hardwiring of the /3PM input. The (/PH1)/STEP output is made active low after a master reset. /3PM is tied high in the MDIO.

Head Load (HLD):

High-level output that controls the loading of the Read/Write Head against the recording medium (diskette). A Read or Write operation do not occur until a high-level HLT input is sampled be the 1771-1. The HLD becomes active at the beginning of a Read, Write (E flag is set high) or Verify operation, or a Seek or Step Operation with the H flag set high; it remains active until the third index pulse following the last operation that used the head.

5 - 8.3 INPUT/OUTPUT SIGNALS

Data Acess Lines (DAL) Bus:

This TRI-STATE bus comprises eight inverted input/output lines (/DAL0 - /DAL7). The bus provides bi-directional communications between the CPU and the 1771-I. Data, control words and status information are transferred via the DAL bus.

5 - 8.4 ELECTRICAL CHARACTERISTICS

DC

TA = 0 degrees C to +70 degrees C.
VDD = +12V +/-0.6V
VBB = -5V +/-0.25V
VSS = 0V
VCC = +5V +/-0.25V

AC

Characteristic (Symbol)	Min	Typ	Max
External Data Separation (/XTDS = 0)			
Pulse Width RD Data & Rd Clock (PWX)	150 ns		350 ns
Clock Cycle Ext (CX)	2500 ns		
Data to Clock (DEX)	500 ns		
Data to Data Cycle (DDX)		2500 ns	
Write Data Timing			
Write Gate to Data (WGD)		1200 ns	
Pulse Width Write Data (PWW)	500 ns		600 ns
Clock to Data (CDW)	2000 ns		
Clock Cycle Write (CW)	4000 ns		
Write Gate Hold to Data (WGH)			100 ns
Miscellaneous Timing			
Clock Duty (CD1)	350 ns (+/-1%)		
Clock Duty (CD2)	210 ns		
Step Pulse Output (STP)	7600 ns		8400 ns
Dir Setup to Step (DIR)	48 us		
Master Reset Pulse Width (MR)	20 us		
Index Pulse Width (IP)	20 us		
Write Fault Pulse Width (WF)	20 us		

5-8.5 CONTROLLER PROCESSES

The following is a complete resume of controller processes for the 1771 MDIO controller device.

COMMANDS

The 1771-1 accepts and executes eleven commands. With the exception of the Force Interrupt command, a command word should be loaded into the internal Command Register only when bit 0 (Busy) of the Status Register is inactive (low). Whenever a command is being executed, the Busy status bit is reset low. The Status Register indicates whether a completed command encountered an error or was fault free.

The eleven commands accepted and executed by the 1771-1 are divided into four types. The following paragraphs describe the eleven commands under these four divisions.

TYPE 1 COMMANDS

Type 1 Commands are basically head positioning commands and include the Restore, Seek, Step, Step-in, and Step-out commands. Each of the Type 1 Commands contains a rate (r1r0) field (bits 0 and 1) that determines the stepping motor rate.

The Type 1 Commands contain a head load (h) flag (bit 3) that determines whether or not the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is high). If h = 0, the HLD output is made inactive low. Once the head is loaded (HLD is active), the head will remain engaged until the 1771-1 receives a command that specifically disengages the head. If the 1771-1 does not receive any commands after two revolutions of the disk, the head will be disengaged (HLD made inactive). The Head Load Timing (HLT) input is only sampled after a 10 millisecond delay, when actual reading or writing on the diskette is to occur. Note that a verification, described below, requires reading off the diskette.

The Type 1 Commands also contain a verification (V) flag (bit 2) that determines whether or not verification is to take place on the last track. If V = 0, no verification is performed. If V = 1, a verification is performed.

During verification, the head is loaded (HLD is active) and after an internal 10 millisecond delay, the HLT input is sampled. When the HLT input is active (high), the first encountered ID field is read off the diskette. The track address of the ID field is then compared to the Track Register. If there is a match and a valid ID CRC, the verificaion is complete, an interrupt is generated, the Busy status bit is reset. If there is not a match and a valid ID CRC, an interrupt is generated, the Seek Error status bit (bit 4) is set high, and the Busy status bit is reset low. If there is not a valid CRC, the CRC Error status bit (bit 3) is set high, and the next encountered ID field is read off the diskette for verification. If an ID field with a valid CRC cannot be found after two revolutions of the diskette, the 1771-1 terminates the operation and sends an interrupt (INTRO) signal to the CPU.

The Step, Step-in and Step-out commands contain an update (u) flag (bit 4).

When u = 1, the Track Register is updated by one for each step. When u = 0, the Track Register is not updated.

Restore (Seek Track 0): Upon receipt of this command, the Track 00 (/TR00) input is sampled. If /TR00 is active low (indicating the Read/Write head is positioned over track 0), the Track Register is loaded with zeros and an interrupt is generated. If /TR00 is not active low, stepping pulses at a rate specified by the r1r0 field (bits 0 and 1) are issued until the /TR00 input is active low. At this time, the Track Register is loaded with zeros and an interrupt is generated. If the /TR00 input does not go active low after 255 stepping pulses, the 1771-1 gives up and interrupts with the Seek Error status bit set. Note that the Restore command is executed when the /MR input goes from an active (low) to an inactive (high) state. A verification operation takes place if the V flag (bit 2) is set. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command.

Seek: This command assumes that the Track Register contains the track number of the current position of the Read/Write head and that the Data Register contains the desired track number. The 1771-1 will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register. A verification operation takes place if the V flag (bit 2) is set. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-in: Upon receipt of this command the 1771-1 issues one stepping pulse in the direction towards track 76. If the u flag (bit 4) is set, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag (bit 2) is set. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of one command.

Step-out: Upon receipt of this command, the 1771-1 issues one stepping pulse in the direction towards track 0. If the u flag (bit 4) is set, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag (bit 2) is on. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE 2 COMMANDS

The Type 2 Commands include the Read sector(s) and Write sector(s) commands. Prior to loading the Type 2 Commands into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type 2 Commands, the Busy status bit is set. If the E flag (bit 2) = 1 (this is the normal case), HLD is made active and HLT is sampled after an internal 10 millisecond delay. If the E flag = 0, the head is assumed engaged and there is no internal 10 millisecond delay.

When an ID field is located on the diskette, the 1771-1 compares the Track Number of the ID field with the Track Register. If there is not a match, the

next encountered ID field is read and a comparison is made. If there is a match, the sector number of the ID field is then compared with the Sector Register. If there is a match, the CRC field is read. If there is a CRC error, the CRC Error status bit is set and the next ID field is read off the diskette and comparisons are made. If the CRC is correct, the data field is located and will be either written or read, depending upon command. The 1771-1 must find an ID field with a valid track number, sector number, and CRC within two revolutions of the diskette; otherwise, the Record Not Found status bit (bit 4) is set and the command is terminated with an interrupt.

Each of the Type 2 Commands contains a b flag (bit 3) which in conjunction with the sector length field contents of the ID, determines the length (number of characters) of the data field. For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128 x 2 to the nth power where n = 0, 1, 2, or 3.

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field.

Each of the Type 2 Commands also contains an m flag (bit 4) that determines whether multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the Sector Register internally updated so that an address verification can occur on the next record. The 1771-1 continues to read or write multiple records and update the Sector Register until the Sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register. When either of these occurs, the command is terminated and an interrupt is generated.

Read Command: Upon receipt of this command, the Read/Write head is loaded and the Busy status bit is set. Then, when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is input to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct ID field. If not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the Data Shift Register, it is transferred to the Data Register and a Data Request (DRQ) output is generated. When the next byte is loaded into the Data Shift Register, it is transferred to the Data Register and another DRQ output is generated provided that the CPU has previously read the Data Register. If one or more characters are lost, the Lost Data status bit is set. This sequence continues until the data field has been input to the computer. If there is a CRC error in the data field, the CRC Error status bit is set, and the command is terminated (even if it is a multiple record command). At the end of the operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (bits 5 and 6).

Write Command: Upon receipt of this command, the Read/Write head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ output is generated. The 1771-1 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the

Data Register has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of all Zero levels are then written on the diskette. At this time, the Data Address Mark is then written on the diskette, as determined by the a1a0 field (bits 0 and 1) of the command as shown below:

a1	a0	Data Mark (hex)	Clock Mark (hex)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

The 1771-1 then writes the data field by generating DRQ outputs to the computer. If the DRQ is not serviced in time, the Lost Data status bit is set and a byte of zeros is written on the diskette. The command is not terminated. After the last data byte has been written on the diskette, the two-byte CRC is computed internally and written on the diskette followed by one byte of all One level. WG is then made active.

TYPE 3 COMMANDS

Read Address: Upon receipt of this command, the head is loaded and the Busy status bit is set. The next encountered ID field is then read in off the diskette, and the six data bytes of the ID field are assembled and transferred to the Data Register, and DRQ output is generated for each byte.

Although the CRC characters are input to the computer, the 1771-1 checks for validity and the CRC Error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the Sector Register. At the end of the operation, an interrupt is generated and the Busy status bit is reset.

Read Track: Upon receipt of this command, the head is loaded and the Busy status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled, it is transferred to the Data Register and the Data Request (DRQ) output is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If the /s flag (bit 0) of the command is a low, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

The 1771-1 handles single density frequency modulate (FM) data. Each data cell is defined by clock pulses. A pulse recorded between clock pulses indicates the presence of a logic 1 bit; the absence of this pulse is interpreted as a logic 0 bit. The Address Marks for Index, ID, and Data are identified by a particular pattern not repeated in the remainder of the ID field or Data field. This is accomplished by reading patterns that are recorded with missing clock bits (logic 0) as shown below:

For initialization:

Write 2 CRC characters

Data	1 1 1 1 0 1 1 1	= F7
Clock	1 1 1 1 1 1 1 1	= FF

Index Address Mark

Data	1 1 1 1 1 1 0 0	= FC
Clock	1 1 0 1 0 1 1 1	= D7

ID Address Mark

Data	1 1 1 1 1 1 1 0	= FE
Clock	1 1 0 0 0 1 1 1	= C7

Data Address Mark

Data	1 1 1 1 1 0 1 1	= F9-FB
Clock	1 1 0 0 0 1 1 1	= C7

Deleted Data Address Mark

Data	1 1 1 1 1 0 0 0	= F8
Clock	1 1 0 0 0 1 1 1	= C7

Spare

Data	1 1 1 1 1 1 0 1	= FD
Clock	(user defined)	

These patterns are used as synchronization codes by the 1771-1 when reading data and are recorded by the formatting command (Write Track) when the 1771-1 is presented with data F7 through FE.

Write Track: Upon receipt of this command, the head is loaded and the Busy status bit is set. Writing starts with the leading edge of the encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request output is activated immediately upon receiving the command and writing does not start until after the first byte has been loaded into the Data Register. If the Data Register has not been loaded by the second index pulse, the operation is terminated. This sets the Not Busy and Lost Data status bits, and activates the interrupt. If a byte is not present in the Data Register when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the diskette by detecting certain data byte patterns in the outgoing data stream as shown above. The CRC generator is initialized to all Ones when any data byte from F8 to FE is about to be transferred from the Data Register to the Data Shift Register.

The Write Track command does not execute if the /DINT input is grounded. Instead, the Write Protect status bit is set and the interrupt is activated. One

F7 pattern in the Data Register generates 2 CRC characters.

TYPE 4 COMMANDS

Force Interrupt: This command can be loaded into the Command Register at any time. If there is a current command under execution (Busy status bit is set), the command is terminated and an interrupt is generated when the condition specified in the I0 through I3 field (bits 0 through 3) is detected. More than one condition may be specified. The interrupt conditions are indicated below:

I0 = Not Ready-to-Ready Transition
I1 = Ready-to-Ready Transition
I2 = Every Index Pulse
I3 = Interrupt occurs within 1 to 10 milliseconds and every 10 milliseconds thereafter.

NOTE: If I0 through I3 = 0, no interrupt is generated; however, the current command is terminated and the Busy status bit is reset.

5-8.6 STATUS REGISTER

An 8-Bit register is provided in the 1771-1 to hold device status information. This Status information varies according to the type of command executed as shown in Table 3. The contents of the Status Register, which can be read into the DAL Bus by a Read operation, are described below.

Bit 0:

When high (set), indicates that a command is under execution. When low (reset), indicates that no command is under execution.

Bit 1:

For Type 1 Commands, this bit is the complement of the Index Pulse (/IP) input. When set, it indicates that an index mark has been detected on the diskette.

For Types 2 and 3 Commands, this bit is a copy of the Data Request (DRQ) output. When set, it indicates that the Data Register is full during a Read operation or that the Data Register is empty during a Write operation. Bit 1 is reset to zero when updated.

Bit 2:

For Type 1 Commands, this bit is the complement of the Track 00 (/TR00) input. When set, it indicates that the Read/Write head is positioned over track 0.

For Types 2 and 3 Commands, this bit is set to indicate the computer did not respond to the DRQ output from the 1771-1 in one byte time. Bit 2 is reset to zero when updated.

Bit 3:

For Type 1 Commands, this bit is set when one or more CRC errors were encountered on an unsuccessful Track Verification operation. Bit 3 is reset to zero when updated.

For Type 2 and 3 Commands, bit 3 is set when an error is found in one or more ID fields, while bit 4 is set. Bit 3 is reset low when updated.

Bit 4:

For Type 1 Commands, this bit is set to indicate that the desired track was not verified. Bit 4 is reset low when updated.

For Type 2 and 3 Commands, bit 4 is set to indicate that the desired track and sector were not found. Bit 4 is reset low when updated.

Bit 5:

For Type 1 Commands, this bit is set to indicate that the Read/Write head is loaded and engaged. Bit 5 is the logical AND of the Head Load (HLD) output and the Head Load Timing (HLT) input.

For Types 2 and 3 Commands, bit 5 indicates the following: the LSB of the record-type code from the data field address mark during execution of a Read Command; and a write fault during execution of a Write or Write Track Command. Bit 5 is reset low when updated.

Bit 6:

For Type 1 Commands, this bit is the complement of the Write Protect (/WRPT) input. When set, it indicates that the write protect is activated.

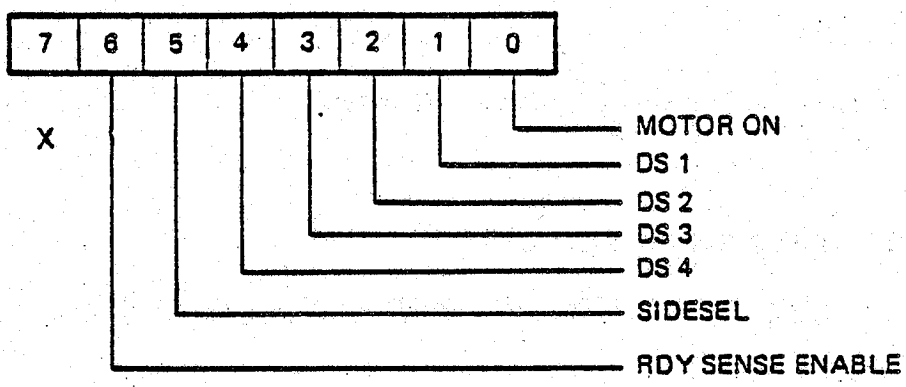
For Type 2 and 3 Commands, bit 6 indicates the following: The MSB of the record-type code from the data field address mark during execution of a Read Command; and a write fault during execution of a Write or Write Track command. Bit 6 is reset low when updated.

Bit 7:

When set, indicates that the floppy disk drive is not ready. When reset, indicates that the drive is ready. Bit 7 is the complement of the Ready input and is logically ORed with the Master Reset (/MR) input. The Types 2 and 3 Commands are not executed unless the floppy disk drive is ready.

5 - 8.7 CONTROL PORT

The memory-mapped port sources the mini drive control lines MOTORON, DS1 - DS4, and SIDESEL. The latter is not used by the MDIO firmware and is always high. Similarly, DS4 is not used by the MDIO firmware and is always low.



5 - 8.8 DATA SEPARATOR

The separator consists of two stages: a synchronization front end, followed by a quadrature circuit. The front end synchronizes the incoming FM pulse stream to the on-board 2 MHz clock. It does this by first converting the pulse stream to an NRZ waveform (U19) then reconstructing the now synchronized pulse stream (U20, U7 and U9). This is traced in waveforms of the Data Separator timing diagram.

Each FM pulse broadsides the 4-bit binary counter (U21) with the value N101, where N is the current binary value of Q(D), the output of the fourth stage of the counter.

In the timing diagram, Q(D) is assumed to be low at the beginning of the first bit-cell shown. It could just as easily have been high, due to asynchronism in bit-timing between the drive output and the separator, but a low is chosen at this time for ease of discussion.

LOADing of the counter will jam the value 1101 into its stages (Q(D) will remain) and the next pulse coming from pin 10 of U20 will be routed to the FDCLOCK line. Three clock cycles later, the counter rolls over and Q(D) toggles, ready now to steer the (possible) next pulse to the FDDATA line.

In the absence of a data pulse, the counter does not get LOADed and, hence, Q(D) will toggle after eight more clock cycles, ready, again, to steer the next pulse to the FDCLOCK line.

By loading the counter on each FM pulse, the quadrature waveform (Q(D)) is updated at least once per bit-frame (and twice during every "1" bit). This ensures tight tracking of the raw FM pulse stream by the data separator.

Note that the 1771-1 is interested in the leading edges of FDCLOCK and FDDATA. While in frequency synchronization, these edges will fall on or near the center of the quadrature waveform which, of course, extends 25% of bit-time back- and forward in time. Considerable pulse jitter can thus be tolerated and changes in pulse separation, between any two consecutive pulses, of nearly 25% of bit-time (i.e., 2 us) will not impair data recovery.

Depending on initial conditions, Q(D) may or may not be in phase synchronization with the FM pulse stream. The separator may, therefore, output data pulses on the FDCLOCK line. This is of no consequence, as the 1771-1 will perform phase synchronization upon

detection of synch sequences consisting of multiple NUL bytes.

5 – 9 MDIO JUMPER CONFIGURATIONS

The following is a complete summary of the MDIO Jumper Configurations and loci.

Address Decoding:

The board is pc'ed for 65K maximum system configuration and the FANTOM line is enabled:

	A14	O – P
	A15	R – S
FANTOM	A16	U – V

For systems with memory configured for more than 65K, these changes in the jumper configuration must be made:

Delete	O – P	Add	P – Q
	R – S		S – T
	U – V		X – Y

The board is pc'ed to power–up in the MDION–stat. To have it come up /MDION, these jumpers are changed:

Delete	L – M	Add	M – N

INBOARD is generated as /INBOARD for 74LS244 use. To change this for 74LS241 use:

Delete	AE – AD	Add	AD – AF

The board is pc'ed for 2K (2716) ROM/EPROM. To change to 1K capacity, change thusly:

Delete	I – K	Add	I – J
	F – H		F – G

5 – 10 MPU–A COMPATIBILITY/OPERATION

Although pc'ed for MPU–B (8085–based microprocessor) operation, the MDIO board may be modified to work with a 8080–based microprocessor. The following jumper should be changed.

Delete	AA – AB	Add	AA – AC

5 – 11 DRIVE–TYPE SELECTION

During initialization, the READY input of the 1771–1 is used to determine which of the two permissible jumpers, AG – AJ and AJ – AH, is installed on the board.

MDIO firmware strobes the control port with a dummy drive–select byte that selects no drive but does turn on drive motor(s). This strobe fires the DRIVE SELECT ONESHOT, while also latching a "0" into 4Q at U23, thus forcing jumper point AG high.

The firmware then examines the 1771–1 status byte for a READY. If it finds a READY, it infers that the board is strapped for MPI B51 drive use and readies the appropriate parameters for step rate and number of tracks per diskette (12ms, 40 tracks). If it finds a NOT READY, it infers that the board is not strapped for MPU B51 use and readies the default parameters (40ms, 35 tracks). All future control bytes strobed into U23 during drive selection activities will have bit 6 set to force a LO at jumper AG.

The MDIO is factory jumpered to the type drive installed (in most cases MPI B51 drives). However, if occasion requires the use of a different drive, refer to the table below for jumper modifications.

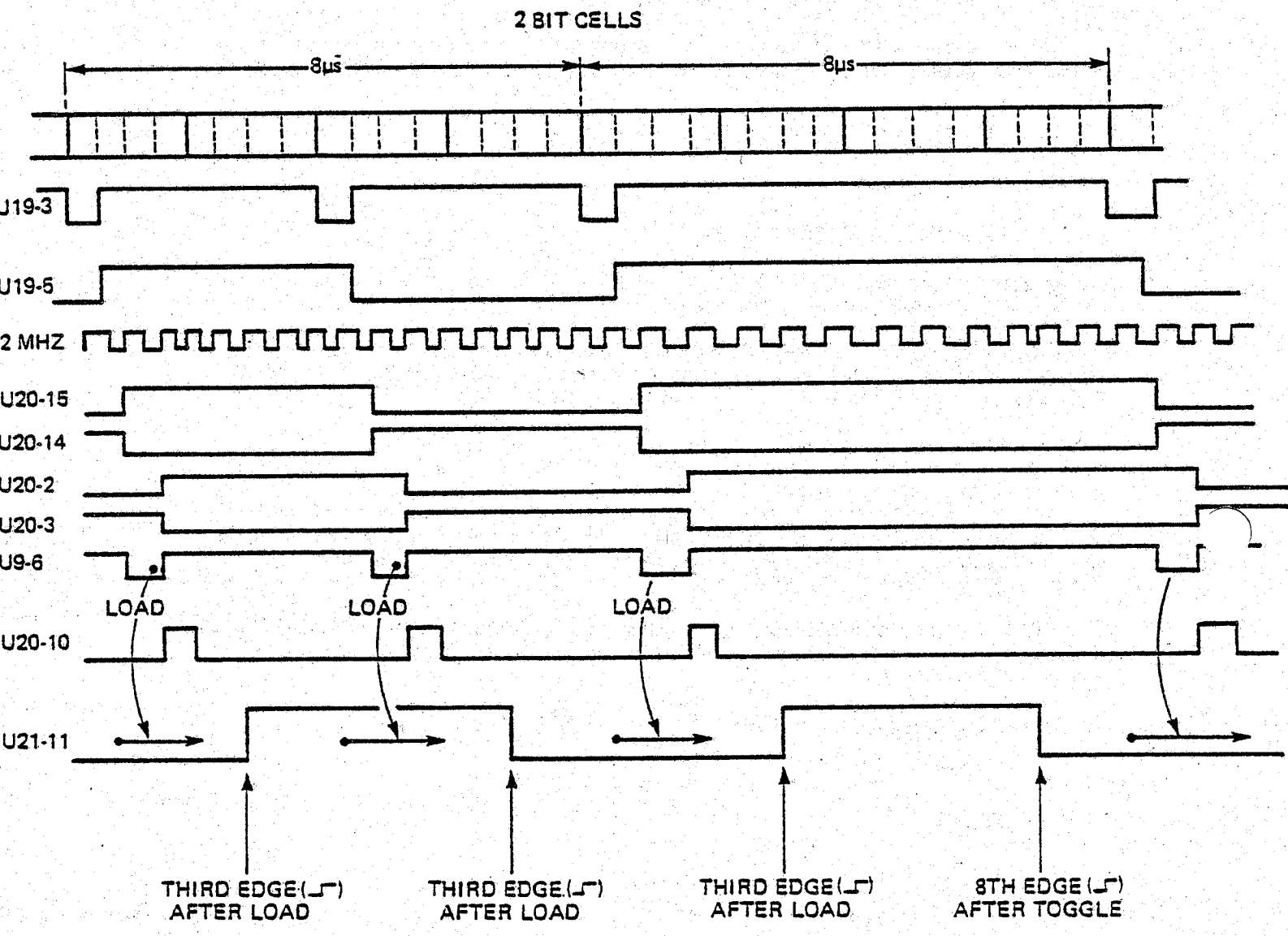
To use a Shugart SA400 or Wangco 82:

Delete	AJ – AH	Add	AJ – AG

To use a Micropolis 1015:

Delete	AJ – AH A – C	Add	AJ – AG A – B

FM DATA SEPARATOR
(AFTER NATIONAL)



- LOAD BROADSIDES N 101 INTO 74161 (WHERE N IS THE CURRENT VALUE OF QD)
- 3 CLOCK PULSES AFTER LOAD, QD TOGGLES.
- IF NO LOAD OCCURS FOR ANOTHER 8 CLOCK PERIODS,
- QP WILL TOGGLE AGAIN

Table 1. Commands Summary

Type	Command	Bits							
		7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\bar{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

Table 2. Command Flags Summary

h = Head Load flag (bit 3 of Type I)

h = 1, Load head at beginning
h = 0, Do not load head at beginning

V = Verify flag (bit 2 of Type I)

V = 1, Verify on last track
V = 0, No verify

r_1r_0 = Stepping Motor Rate (bits 1 - 0 of Type I)

r_1r_0 = 00, 6 ms between steps
r_1r_0 = 01, 6 ms between steps
r_1r_0 = 10, 10 ms between steps
r_1r_0 = 11, 20 ms between steps

u = Update flag (bit 4 of Type I)

u = 1, Update Track Register
u = 0, No update

m = Multiple Record flag (bit 4 of Type II)

m = 0, Single Record
m = 1, Multiple Records

b = Block Length flag (bit 3 of Type II)

b = 1, IBM format (128 to 1024 bytes)
b = 0, Non-IBM format (16 to 4096 bytes)

E = Enable HLD & 10 ms delay (bit 2 of Type II)

E = 1, Enable HLD, HLT & 10 ms delay
E = 0, Head is assumed engaged & no 10 ms delay

a_1a_0 = Data Address Mark (bits 1 - 0 of Type II)

a_1a_0 = 00, FB (Data Mark)
a_1a_0 = 01, FA (Data Mark)
a_1a_0 = 10, F9 (Data Mark)
a_1a_0 = 11, F8 (Data Mark)

$\bar{s}$ = Synchronize flag (bit 0 of Type III)

$\bar{s}$ = 0, Synchronize to AM
$\bar{s}$ = 1, Do not synchronize to AM

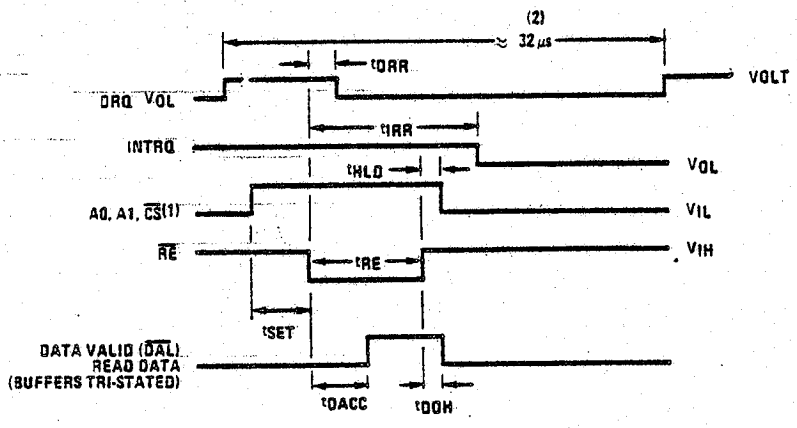
I_n = Interrupt Condition flags (bits 3 - 0 of Type IV)

I_0 = 1, Not Ready to Ready Transition
I_1 = 1, Ready to Not Ready Transition
I_2 = 1, Index Pulse
I_3 = 1, Every 10 ms

Table 3. Status Register Summary

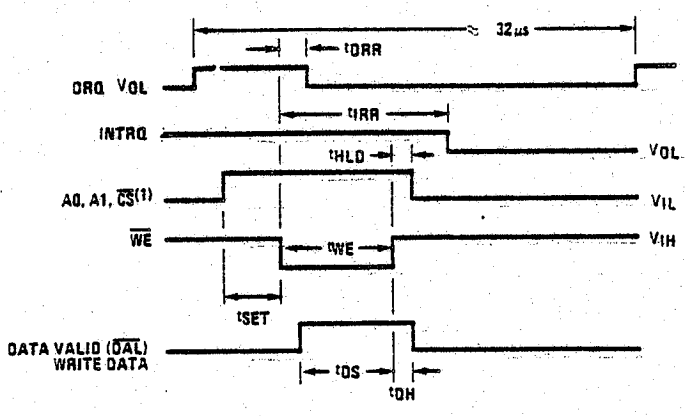
Bit	Commands					
	All Type I Commands	Read Address	Read	Read Track	Write	Write Track
S7	Not Ready	Not Ready	Not Ready	Not Ready	Not Ready	Not Ready
S6	Write Protect	0	Record Type	0	Write Protect	Write Protect
S5	Head Engaged	0	Record Type	0	Write Fault	Write Fault
S4	Seek Error	ID Not Found	Record Not Found	0	Record Not Found	0
S3	CRC Error	CRC Error	CRC Error	0	CRC Error	0
S2	Track 0	Lost Data	Lost Data	Lost Data	Lost Data	Lost Data
S1	Index	DRQ	DRQ	DRQ	DRQ	DRQ
S0	Busy	Busy	Busy	Busy	Busy	Busy

ing Waveforms



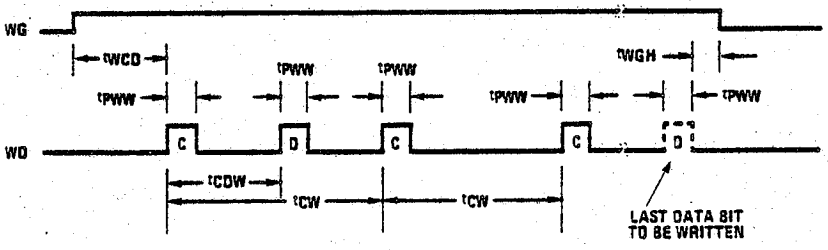
NOTES:
1. /CS may be permanently tied low if desired.
2. For read track command, this time may be 24 to 64 us.

Read Enable Timing

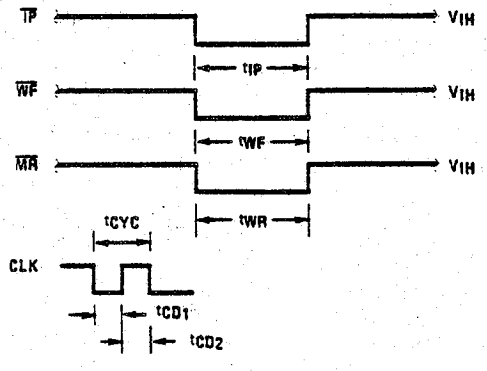


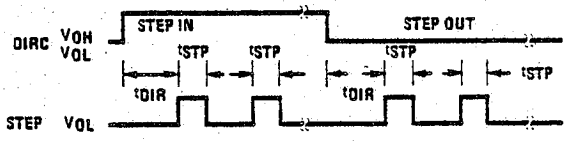
NOTES:
1. /CS may be permanently tied low if desired.
2. When writing data into sector, track, or data register, user cannot read this register until at least 16 us after the rising edge of /WE. When writing into the command register, status is not valid until some 24 us later. These times are doubled when CLK =1 MHz.

Write Enable Timing



Write Data Timing





Miscellaneous Timing

006560
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74LS123
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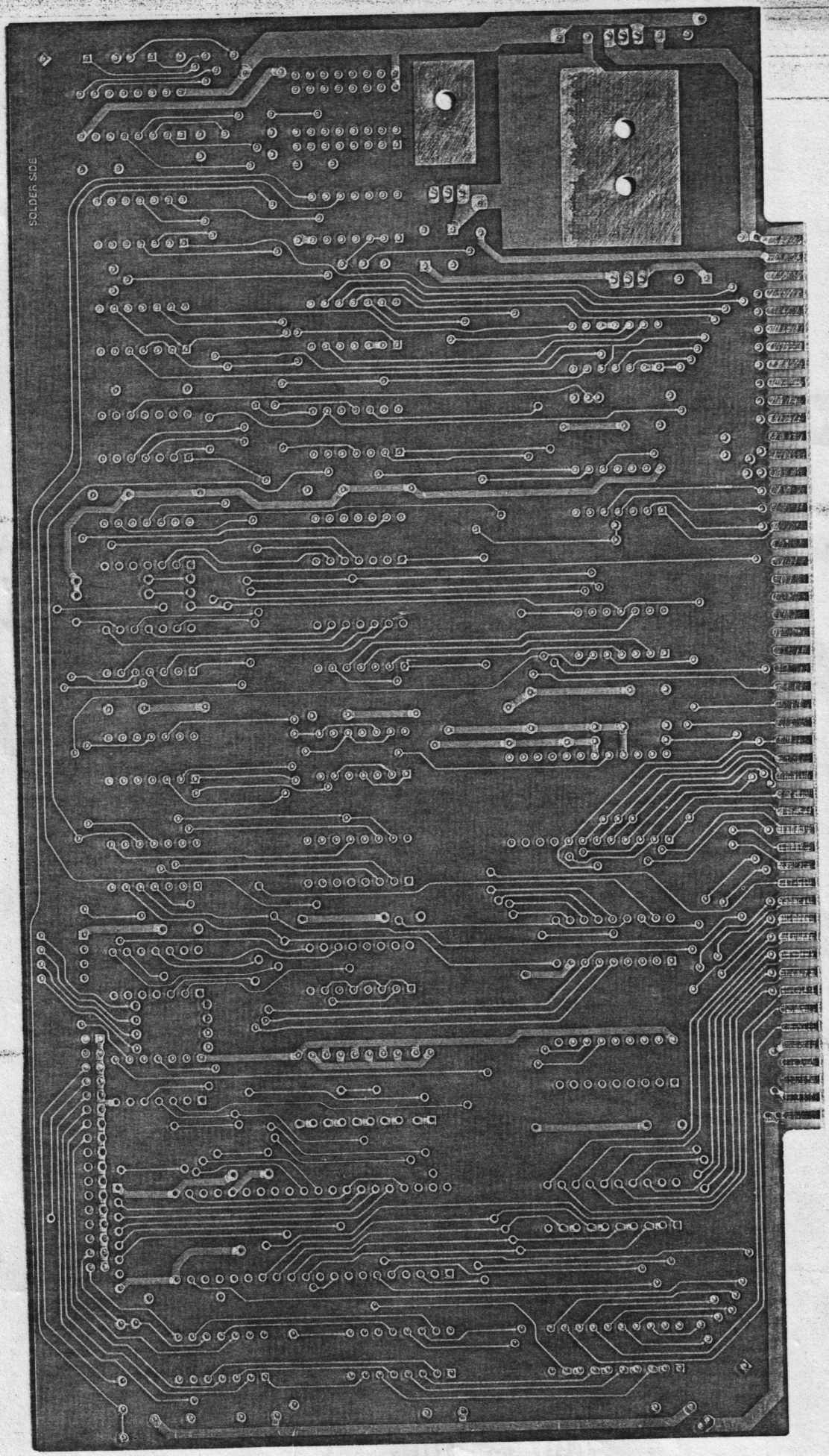
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